THE NATIONAL INSTITUTE OF ENGINEERING
Manandavadi Road, Mysuru

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

PROCEEDINGS OF THE BOARD OF STUDIES (BOS)
13/08/2020
NIE, Mysore
13/08/2020
MEMBERS OF THE BOS MEETING

<table>
<thead>
<tr>
<th>Chairperson</th>
<th>Dr. Narasimha Kaulgud, Professor and HOD</th>
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</thead>
<tbody>
<tr>
<td>Members</td>
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</table>
| Faculty members at different levels covering different specialization. | 1. Dr. Rohini Nagapadma  
2. K V Nagalakshmi  
3. Dr. Shashidhara H R  
4. Dr. S Parameshwara  
5. Dr. C Anjanappa |
| Members     |                                           |
| Two experts in the subject from outside the College. | Raghupathi S, Tech. Leader, CISCO Systems Bengaluru  
9845531150  
ragraghu@cisco.com |
| Members     |                                           |
| One expert from outside the College, to be nominated by the Vice Chancellor, VTU, Belgaum | Dr. Rudraswamy, Professor, Dept. of ECE, SJCE, Mysuru  
Mob: 8861020598  
rudra.swamy@sjce.ac.in |
| Member      |                                           |
| One representative from industry / corporate sector / allied area relating to placement. | Dr. B Kanmani, Prof, and Head, Dept of Telecommunication, BMS college of Engg., Bengaluru.  
Mob: 9448375397  
bkanmani.tec@bmsc.ac.in |
| Member      |                                           |
| One postgraduate meritorious alumnus, to be nominated by the Principal. | Dr. Sujatha Jaganath, Wipro, Bangalore  
Ph.No.9686571281  
E-Mail: sujatha.jaganath@wipro.com |
| Member      |                                           |
| One postgraduate meritorious alumnus, to be nominated by the Principal. | Dr. Naveen, Professor, Dept. of Electrical Engineering IIT, Dharwad. Ph:8861021944  
E-mail: naveenmb@iitdh.ac.in |
DEPARTMENT OF E&C
BOS MEETING

AGENDA
1. Discussion regarding PO attainment for the year 2018-19
2. Suggestions from DIAB, DAAB board.
3. Suggestions from NBA.
4. Suggestions from Alumni and Employer survey feedback
5. Suggestions from Parent and Student feedback.
6. Blown up syllabus of 4\textsuperscript{th} year of UG as per curriculum 2017-18
7. Blown up syllabus of 3\textsuperscript{rd} year of UG as per curriculum 2018-19
8. Blown up syllabus of 2\textsuperscript{nd} year of UG as per curriculum 2019-20.
9. Blown up syllabus for 1\textsuperscript{st} year of UG as per curriculum 2020-24.
10. Scheme & syllabus of all semester of M.Tech courses “Networking and Internet Engineering” as per curriculum 2020-22.
11. BoS Minutes of meeting.
12. Any other academic matters.
**Agenda 1:** Discussion regarding PO attainment for the year 2018-19.

- No Comments.

**Agenda 2:** Suggestions from DIAB & DAAB members

1. Students as to be advised to take up MOOC elective which helps them to execute mini projects.
2. In DSP subject, instead of bilinear transformation include lattice based Digital IIR and FIR filters.
4. For Control systems subject, Include textbooks like Nagoor Kani, Ganesh Rao for better understanding.
5. For Control systems Subject, practical examples and cases to be included in the syllabus.
6. Engineering Management as to be introduced before 7th sem, it will be helpful for placement activities. Introduce more of case studies and assignments.
7. DSP laboratory: introduce optimization codes (O3 levels).
8. Include societal driven subjects like EM and RF Compatibility and Provision for interdepartmental electives.
10. For Communication Networks introduce concepts of Wireshark in theory sessions.
11. Explore the possibility of addition of experiments on Optical networks, Mobile Communication and Satellite Communication.
12. Concepts on large scheduler and RTOS hands on as to be included.
14. Encourage students to publish SCI journals and assign credits to it.
16. In SLE components include introduction to Industrial IoT kits.
17. Neural Networks: Include Elements of Artificial Neural Networks.
18. Involve students in Panel discussions, Enlighten them regarding product development cycle and analysis of practical problems.

**Agenda 3:** Suggestions from NBA.

1. Increase the number of SCI publications.
2. Improvement required in funded projects.

**Agenda 4:** Suggestions from Alumni and Employer survey feedback

1. Analog VLSI need to be added in the curriculum.
2. More emphasis on FPGA.
3. Neural Network, Database, AI, Machine Learning should be included.
4. EMFT, Parallel and Distributed Computing Algorithms, subjects must be included.
5. Lack in leadership qualities.
**Agenda 5:** Suggestions from Parent and Student feedback.
1. More Industry based Education.
3. Include 5G wireless courses.
4. Include hardware implementation in DSP.
5. More practical Exposure.

**Agenda 6:** Blown up syllabus of 4th year of UG as per curriculum 2017-18.
- No Change

**Agenda 7:** Blown up syllabus of 3rd year UG as per curriculum 2018-19
- Blown up syllabus of 3rd year UG as per curriculum 2018-19 has been approved by BoS members.
  a. New MOOC electives of 3rd credits were introduced for 5th semester.
     i. Joy of computing with python
     ii. Digital VLSI testing
  b. New MOOC value added electives were introduced for 5th semester.
  c. CMOS VLSI and Embedded System LTP structure swapped.
  d. Embedded System laboratory got replaced with CMOS VLSI Laboratory and Embedded Systems experiments will be conducted in tutorials.
  e. “Advanced Communication” and “Information and coding theory” got merged and renamed as Communication System and Coding Theory.
### Scheme and Syllabus of III Year UG Programme

#### SCHEME OF TEACHING AND EXAMINATION

##### V SEMESTER

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**Total Credits** 24

**Total Contact Hrs** 29

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#### SCHEME OF TEACHING AND EXAMINATION

##### VI SEMESTER

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**DIGITAL SIGNAL PROCESSING (3:2:0)**

**Sub. Code:** EC5C01

**CIE:** 50% Marks

**Hrs /Week:** 3

**SEE:** 50% Marks

**SEE Hrs:** 3 Hrs

**Max. Marks:** 100

**Pre-requisite:** Signals and Systems (EC4C05)

**Course Outcome:**

On successful completion of the course, the students will be able to

1. Analyze signals using various Transforms.
2. Apply an efficient DFT in linear filtering methods.
3. Design IIR and FIR filters relative to specific performance parameters.
4. Understand architecture for DSP applications - TMS32067x processor.

**Unit 1: Discrete Fourier Transform (DFT) & Properties of DFT:**

Frequency domain sampling and reconstruction of discrete-time signals, Discrete Fourier Transform (DFT), DFT as a linear transformation, relationship of the DFT to other transforms. **Properties of the DFT:** linearity, periodicity, multiplication of two DFTs, circular convolution, and symmetry properties, frequency analysis of signals using the DFT.

9 Hrs

**SLE:** Additional DFT Properties.

**Unit 2: Fast Fourier Transform Algorithms:**

SLE: Chirp Z-Transform.

Unit 3: Design and Realization of FIR Filters:
Properties of FIR digital filters, different types of windows - Rectangular, Hanning, Hamming, design of FIR filters using above windows.

**Realization of FIR filter structures** - Direct form structure, linear phase and cascade FIR structure. 9 Hrs

SLE: Design of Blackmann & Kaiser windows, MATLAB programming for above windows.

Unit 4: Design and Realization of IIR Filters:
Frequency transformations in the analog domain, characteristics of commonly used analog filters, IIR filter design by impulse invariance method, Bilinear transformation, application of above technique to the design of Butterworth & Chebyshev filters.

**Realization of IIR Filter Structures**: Direct forms (I & II), cascade and parallel realizations, 9 Hrs

SLE: Comparison of IIR & FIR digital filters, Matched-transformation,

Unit 5: Digital Signal Processors: Architectural features of a Digital Signal Processor, fixed point and floating point processors, different generations of DSPs, TMS 320C67X processors. (Text2) 6 Hrs

SLE: Fixed point arithmetic.

Text Books:


Reference Book:

DIGITAL DESIGN USING VERILOG  (3:2:0)

Sub Code: EC5C02          CIE: 50% Marks
Hours /Week: 3              SEE: 50% Marks
SEE Hrs.: 3                 Max. Marks: 100

Pre-requisite: Digital System Design (EC3C02)

Course Outcome:
On successful completion of the course, the students will be able to:

● Describe Verilog language syntax, semantics and write Verilog programs and model them in different levels of Abstraction.

● Design and verify the digital circuit by mean of Computer Aided Engineering tools which involves programming with the help of Verilog HDL.

● Simulate, synthesize, and program their designs on a development board.

● Design, verify and implement PLI and FSM to control complex systems

Module 1: Fundamentals of Verilog and FPGA architectures:  Introduction, FPGA and ASIC Design Flow, Design Methodologies, examples for design methodologies, FPGA Architectures, CLB Design for different logic circuits, basics on IO design, Modules.

6 Hours

SLE: Introduction to simulation tools

Module 2: Basic Verilog Constructs and Dataflow Modelling:

Lexical Conventions, Data Types, System Tasks and Compiler Directives, Modules, Ports, Hierarchical Names, Gate Types, Switch Level Modelling, Gate Delays, Continuous Assignments, Delays, Expressions, Operators and Operands, Operator Types, Examples, Verilog HDL Synthesis: Verilog Constructs, Verilog Operators.

8 Hours

SLE: Exploring open source EDA tools for different level modelling through Verilog codes

Module 3: Behavioral Modelling:

Structured Procedures, Procedural Assignments, Timing Controls, Conditional statements, Multiway Branching, Loops, Sequential and Parallel Blocks, ROUTING structure of conditional control constructs, Parameter and Constant, Design examples for Combinational
and Sequential circuits, Testbench, Case study, Interpretation of a Few Verilog Constructs, Example of Sequential circuit synthesis.

**10 Hours**

**SLE:** Programming using Mixed Style of Verilog modelling

**Module 4: Tasks, Functions and Advanced constructs:**

Tasks, Functions, Differences Between Tasks and Functions, Procedural Continuous Assignments, Overriding Parameters, Conditional Compilation and Execution, Time Scales, Useful System Tasks, Timing and delays, Verification of Gate-Level Netlist.

**8 Hours**

**SLE:** Programming using User Defined Primitives

**Module 5: PLI and FSM based design:** Programming Language Interface, Mealy and Moore outputs, FSM code development, design examples, Introduction – FSMD, Code development of an FSMD, Design examples, Example of Sequential circuit FSM synthesis.

**8 Hours**

**SLE:** ASM Charts

**Text book:**


**Reference Books:**

LIST OF EXPERIMENTS

PART A: Simulation, Synthesis and Implementation using Vivado and Artix 7/Zynq 7 Developmental Boards. Verifying and optimizing the design by analysing the CLB’s and I/O’s for the given FPGA board.

1. Logic gates in Structural, Dataflow and Behavioral
2. Combinational Circuits 1
3. Combinational Circuits 2
4. Sequential Circuits 1
5. Sequential Circuits 2

PART B: Simulate and Synthesis following circuit by HDL based design entry using Cadence tool (ASIC flow)

6. Combinational Circuits 1
7. Combinational Circuits 2
8. Sequential Circuits 1
9. Sequential Circuits 2
10. Implementation of FSM

Text book:


ANALOG & DIGITAL COMMUNICATIONS (4:0:0)

Sub. Code: EC5C03
Hrs/Week: 4
CIE: 50% Marks
SEE: 50% Marks
SEE Hrs: 3
Max. Marks: 100
Course Outcomes:

On successful completion of the course, the students will be able to

1. Describe and analyze the working of amplitude and frequency modulated systems.
2. Describe different types of noise, evaluate noise figure and figure of merit for various communication systems.
3. Distinguish between Analog and Digital Communication systems and analyze various sampling methods and its reconstruction.
4. Analyze and solve problems on various waveform coding and baseband shaping techniques.
5. Describe and analyze various modulation schemes in digital communication systems and solve problems on probability of error.

Module 1: Analog Modulation:


11Hrs.

SLE: Vestigial Side-Band Modulation, FM Broadcast receivers.

Module 2: Noise & Noise in Continuous wave modulation systems:

Introduction, thermal noise, white noise, Noise equivalent bandwidth, Noise Figure, noise effect in two-port networks. Noise performance in AM and FM receivers, Pre-emphasis and De-emphasis.

7 Hrs.

SLE: Noise Reduction Techniques

Module 3: Sampling Process:

Introduction, Basic signal processing operations in digital communication, Sampling and Sampling Theorem: Ideal, natural and flat top sampling, Quadrature sampling of Band pass signal, TDM

8 Hrs.

SLE: Design of flattop sampling circuit.

Module 4: Waveform Coding Techniques:

PCM, Quantization, Quantization noise and SNR, robust quantization, DPCM, DM. 8 Hrs.

SLE: ADPCM and its applications.

Module 5: Base-Band Shaping for Data Transmission:
Discrete PAM signals, ISI, Nyquist’s criterion for distortion less base-band binary transmission, correlative coding, eye pattern, base-band M-ary PAM systems, equalization.  

**7 Hrs.**

**SLE: Adaptive equalization**

**Module 6: Digital Carrier Modulation Schemes:**

Introduction, Binary ASK, PSK, DPSK, FSK, and QPSK modulation schemes, Probability of error, Matched filter and its transfer function, correlator. Comparison of digital modulation schemes **9 Hrs.**

**SLE: SDR.**

**Text Book:**


**Reference Books:**


**CONTROL SYSTEMS (3:0:0)**

**Sub. Code: EC5C04**

**CIE: 50% Marks**

**Hrs. /Week: 3**

**SEE: 50% Marks**

**SEE Hrs: 3 Hrs**

**Max. Marks: 100**

**COURSE OUTCOMES**

1. Determine the time domain specifications for first and second order systems
2. Determine the stability of a system in the time domain and frequency domain
3. To be able to analyze and design PI, PD and PID controllers and to analyze state variables in discrete domain
4. To be able to analyze Discrete systems and understand various applications of control system.
Module 1: Control Systems basic Concepts and Time Response of Feedback Control Systems:

Introduction to Control Systems, Introduction to Block diagrams and signal flow graphs
Time Response of feedback control systems: Standard test signals, Unit step response of First and Second order Systems. Time response specifications, Time response specifications of second order systems, steady state errors and error constants. 8hrs

SLE: Multi input – Multi output control systems, Design considerations of higher order systems.

Module 2: Stability Analysis of Control Systems and Frequency Domain Analysis


SLE: Design considerations of higher order systems and performance indices

Module 3: Design in Control Systems

The design Problem, Preliminary Considerations of classical Design, Realization of Basic Compensators, Tuning of PI, PD and PID Controllers 8hrs

SLE: MATLAB implementation of PID controllers

Module 4: Design of Digital Control System


SLE: Digital Position Control System, Digital Temperature Control System

Module 5: Applications of Control Systems in Electronics

Pole and Zero analysis of a MOS transistor for amplifier designs, Electronic Controller Unit design for process instrumentation and Automotive, Applications of Control System in Processor Design and stability analysis, Control System algorithms for networks and data analytics. 8hrs

SLE: Control System Applications for Augmented and Virtual Reality

Note: Some of the SLE components are implemented in MATLAB/SCILAB

TEXT BOOKS:


REFERENCES:


Control System Laboratory: (Suggested Experiments to be included in DSP Laboratory)

1. Familiarization with MATLAB control system toolbox, MATLAB/ Simulink Toolbox.

2. Determination of step & impulse response for a first order unity feedback system.

3. Determination of step & impulse response for a second order unity feedback system.


5. Determination of bode plot using MATLAB control system toolbox for 2nd order system & obtain controller specification parameters.


7. Determination of Nyquist plot using MATLAB control system toolbox.

8. Analyze the effect of P, PI, PD and PID controllers on a control system.

MOOC – Elective:

1. Joy of computing with python (3:0:0)

   Link: https://onlinecourses.nptel.ac.in/noc20_cs83/

2. Digital VLSI testing (3:0:0)
MOOC–NPTEL Value added courses

1. Robotics
   Link: https://onlinecourses.nptel.ac.in/noc20_de11/preview

2. Scientific computing using Matlab
   Link: https://onlinecourses.nptel.ac.in/noc20_ma40/preview

3. Managerial economics
   Link: https://onlinecourses.nptel.ac.in/noc20_mg67/preview

4. Linear algebra
   Link: https://onlinecourses.nptel.ac.in/noc20_ma54/

Engineering Management (3:0:0)

Sub. Code: EC5C06
CIE: 50% Marks
Hrs. /Week: 3
SEE: 50% Marks
SEE Hrs: 3 Hrs
Max. Marks: 100

Course Outcome:
On successful completion of the course, the students will be able to

1. Explain concepts of Management and its functions.
2. Explain Organisations and Ownership types.
3. Understand Human resource development in organisations.
4. Describe product development life cycle and marketing of products.
5. Explain Project management and the tools used.

Module 1: Management and Functions of Management:
Concept of management, Management, organization, Administration- Taylors Scientific Management - Functions of management- Planning, Organizing, Staffing, Directing, Coordinating, Reporting and Budgeting, Engineers as managers/leaders. 10 Hours
SLE: Leadership types, Manager vs Leader, Management Schools of thought

**Module 2: Organisational Structure and Ownership Types:**
Organisation definition, different types of organisations – Functional, Divisional, Matrix etc.,
Ownership types – Proprietorship, Partnership, LLP, Pvt Ltd, Public Ltd, Section 8 company etc.

8 hours

SLE : Societies, Not for profit Organisations, Trusts

**Module 3: Human Resource and Behavioural management:**

8 Hours

SLE : Other popular motivational theories, Staffing, Employment policies.

**Module 4: Product Development and Marketing**
Product Development Life Cycle, Innovation -Managing and protecting, IPR Concepts, Product positioning,
Marketing – Selling vs Marketing, 4 Ps of marketing, case studies.


8 Hours

**Module 5: Project Management:**
Basic concepts, what is Project. what are the key factors – Time , cost Quality and Scope, Iron Triangle model, Tools used in Project management, Network diagrams, Critical Path method, Quality concepts and 7 Q C Tools.

SLE: PERT, TQM, Project failures

10 Hours

**Text Book:**


**Reference:**


COMMUNICATION LABORATORY (0:0:3)

Sub. Code: EC5L01

Hrs./Week: 3

Course Outcome:

1. Performance Analysis of various modulation techniques and communication circuits.
2. Simulate, and experimentally verify Sampling theorem.

List of Experiments:

1. Test tuned amplifier, find centre frequency, bandwidth and quality factor.
2. Performance analysis of AM and Detection.
3. Performance analysis of FM and Detection.
4. Design and Test a T, π, Bridge and Lattice type Attenuators for a given characteristic resistance and attenuation factor.
5. Verification of Sampling theorem using natural sampling and flat-top samples.
6. Performance Analysis of TDM.
7. Generate PAM for different modulating signals and demodulate using suitable filters.
8. Performance Analysis of ASK and FSK.
9. Performance Analysis of PSK and DPSK.

DIGITAL SIGNAL PROCESSING LABORATORY (0:0:3) – 1.5

Sub. Code: EC5L02

Hrs./Week: 3

Course Outcome:

1: Design and implementation of Signal Processing algorithms for applications in control systems and Signal Processing.

I LIST OF EXPERIMENTS USING MATLAB / SCILAB / OCTAVE / WAB

1. Verification of sampling theorem.
2. Impulse response of a given system
3. Linear convolution of two given sequences.
4. Circular convolution of two given sequences
5. Solving a given difference equation.
6. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum.
7. Design and implementation of FIR filter to meet given specifications.
8. Design and implementation of IIR filter to meet given specifications.

II LIST OF EXPERIMENTS USING DSP PROCESSOR

1. Linear convolution of two given sequences.
2. Circular convolution of two given sequences.
3. Computation of N-Point DFT of a given sequence
4. Realization of an FIR filter (any type) to meet given specifications. The input can be a signal from function generator
5. Realization of an IIR filter (any type) to meet given specifications. The input can be a signal from function generator

Text Book:


CMOS VLSI DESIGN(3:0:0)

Sub. Code: EC6C01
Hrs./Week: 3
SEE Hrs: 3 Hrs

CIE: 50% Marks
SEE: 50% Marks
Max. Marks: 100

Course Learning Outcomes

On successful completion of the course, the students will be able to:

1. Explain VLSI design flow, various inverter schematic and fabrication process.
2. Explain physical design process of VLSI design flow and design rules and layout diagram
3. Explain CMOS process enhancement and delay analysis
4. Design of various CMOS dynamic logic circuits and Adders, Multipliers
5. Explain various VLSI testing and verification methods

Module 1: Fundamentals of VLSI design and Fabrication

VLSI Design Flow, Y chart, CMOS inverter-DC characteristics, Static Load MOS inverters, Differential Inverter, Transmission gate, Tristate Inverter, BiCMOS inverter, Fabrication:
Wafer Processing, oxidation, Epitaxy, deposition, Ion-implantation and Diffusion, Silicon gate process, n-well & p-well process, Twin-tube process.

8 Hrs

SLE: Exploration circuit simulation tool, Inverter (different configuration) schematic design and simulation
Module 2: Layout and circuit design

MOS layers, Stick diagrams, design rules and layout, layout diagrams, symbolic diagrams, examples of layout and stick diagrams of different circuits, NAND and NOR gates, complex logic gates and layout, CMOS standard cell design, switch logic, gate logic.

8 Hrs

SLE: Exploration of layout simulation tool, Inverter (different configuration) layout design and simulation

Module 3: CMOS Process enhancements

CMOS Process enhancements, Resistance, capacitance and inductance estimation, Scaling models and scaling factors, scaling factors for device parameters, limitations of scaling, Latch up problems, The delay unit, Inverter delay, driving large capacitive loads, propagation delays, wiring capacitance, switching characteristics, CMOS gate transistor sizing, power dissipation.

8 Hrs

SLE: Extraction of electrical components, analysis of area, power, timing and back annotation.

Module 4: Subsystem Design

CMOS logic structures: dynamic CMOS logic, clocked CMOS logic, CMOS domino logic, NP domino logic, CVSL, examples of structured design, some clocked sequential circuits. System Design: Structured Adders and Multipliers (CSA, CLA, Tree adders, Booth Multipliers, BG Multiplier and Wallace tree Multipliers)

10 Hrs

SLE: Design and implement of other circuits using TG, pass transistor and other configurations.

Module 5: VLSI testing and Verification

Need for testing, Manufacturing test principles: Fault Models, Fault coverage, ATPG, design strategies for test: DFT, Ad-Hoc testing, scan based test techniques, self-test techniques, IDDQ testing, Design verification algorithms.

6 Hrs

SLE: Exploration of test vectors for different digital circuits through ATPG techniques.

Text books:


Reference Books:

COMMUNICATION SYSTEMS AND CODING THEORY (3:0:0)

Sub. Code: EC6Cxx CIE: 50% Marks
Hrs /Week: 3 SEE: 50% Marks
SEE Hrs: 3 Max. Marks: 100

Course Outcomes:

On successful completion of the course, the students will be able to

- Describe and analyze various modulation schemes in a digital communication system.
- Describe various Digital Communication Techniques.
- Analyze and solve problems on source and channel coding techniques.
- Analyze and solve problems on channel coding schemes.

Module 1: Spread Spectrum Modulation

Pseudo noise sequences, notion of spread spectrum, direct sequence spread spectrum with coherent binary PSK, frequency hopped spread spectrum, applications. 8 Hours

SLE: Role of spread spectrum modulation in CDMA

Module 2: Communication techniques

M-ary FSK: Description, generation, detection, QAM-16: Analysis, generation, MSK: Analysis, generation, detection, GMSK, MIMO: Definition, working, OFDM: Definition, working, Cognitive Radio Technology: Definition, Working. 9 Hours

SLE: QAM-64

Module 3: Information theory and Source Coding Techniques

Introduction, Measure of information, concept of Entropy for memory less sources, Shannon’s encoding algorithm, Shannon-Fano encoding algorithm, Huffman coding, Mutual information, Channel Capacity theorem. 9 Hours

SLE: Binary symmetric and Noiseless channels

Module 4: Channel Coding Techniques- I

Introduction, Linear block codes: Matrix description, error detection and correction, Hamming codes: description, Hamming bound, error detection and correction, Convolution codes (time domain approach only): Calculation of generator sequence, generator matrix, code vector,
Cyclic codes: Systematic and non-systematic cyclic code vectors. Generator and parity check matrices, encoding diagram. 

9 Hours

**SLE: CRC Codes**

**Module 5: Channel Coding Techniques - II**

Reed Solomon Codes: Parameters, calculation of code words and nearest neighbours, applications, Golay codes: Hamming bound, generator polynomial, encoder circuit, BCH codes: code parameter, generator polynomial, Error Correction Capability, Viterbi codes, Trellis codes: Trellis diagram, calculation of encoder output sequence.  

7 Hours

**SLE: Irregular codes.**

**Text Books:**

(http://www.isiweb.ee.ethz.ch/archive/massey_scr/adit1.pdf)

**References:**


**COMMUNICATION NETWORKS (3:2:0)**

**Sub Code:** EC6C03  
**Hrs/Week:** 3  
**SEE Hours:** 3Hrs  
**CIE:** 50% Marks  
**SEE:** 50% Marks  
**Marks:** 100

**Course Outcome:**

On successful completion of the course, the students will be able to:

1. Explain OSI and TCP/IP Protocol Stack, the Transmission Delays, correlation between Data Transmission delay and Propagation Delay.
2. Understand basics of Data Link Layer control, deciphering data using suitable protocols.
3. Design different Networks, Class addresses, subnet and subnet masking.
4. Analyze switching and different routing protocols
5. Implement communication protocols using TCP/UDP in network applications.

**Module 1: Introduction: Network Models and Physical Layer:**

Layers in OSI Model, TCP/IP protocol suite, Addressing, Data Rate Limits, Performance Parameters, Bandwidth, Latency, Switching  
**7hrs**

**SLE:** Application Performance Needs.

**Module 2: Data Link Layer:**

Framing, Flow and Error Control, Protocols, Noiseless Channels, Noisy Channels, HDLC, Random Access, Controlled Access, Wired LANs: Ethernet, Wireless LANs (IEEE 802.11), Bluetooth, Intro to WiMax, Cellular Telephony (1G – 5G)  
**8hrs**

**SLE:** PPP

**Module 3: Network Layer**

**10hrs**

**SLE:** ICMP, IGMP

**Module 4: Transport Layer**

Process to process delivery, UDP, TCP, SCTP(Brief), Data Traffic, Congestion, Congestion Control, Examples  
**8hrs**

**SLE:** QoS, Techniques to Improve QoS

**Module 5: Application Layer**

Client/Server Programming Concept, Domain Name System, SSH, SFTP, SMTP, POP, WWW, HTTP  
**7hrs**

**SLE:** SNMP

**Text Books:**


Reference Books:


EMBEDDED SYSTEMS (3:0:2)

Sub. Code: EC6C04 CIE: 50% Marks
Hrs./week: 3 SEE: 50% Marks
SEE Hrs.: 3 Max Marks: 100

Course Outcome:

On successful completion of the course, the students will be able to:

1. Describe characteristics of embedded systems, design flow, design concepts and Common software components used in embedded system design.
2. Describe Hardware building blocks of an embedded system, performance pertaining to memory and interfacing of an embedded system.
3. Explain different Real Time Operating System standards pertaining to RTOS and performance guidelines.
4. Configuring device drivers and different types of device drivers.

Module 1: Fundamentals of Embedded Systems:

An Embedded System-Definition, Characteristics of Embedded systems, Embedded system Model, Embedded system design Cycle and Development Lifecycle Model, design flow-Hardware-software codesign, software/Hardware components, Real time systems, Hard and Soft RTS, Deadline concepts. 7 Hours.

SLE: Exploring different simulation and Implementation embedded tools.

Module 2: Embedded Linux System:

Boot Loader, Cross compiler, RFS, System Design, Booting Linux, the main software utility tool, Translation tools, debugging tools, testing on host machine, simulators and Laboratory tools. 8 Hours.

SLE: NFS, DHCP.

Module 3: Embedded Hardware:
Embedded hardware building blocks, Structural units in a processor, Processor selection for an embedded systems, Memory selection of an embedded system, Allocation of memory, DMA, Interfacing processor, Memories, and I/O devices, Timers and counting devices, Serial and parallel communication devices, processor performance.  9 Hours.

SLE: optimization of memory needs.

**Module 4: RTOS:**

Introduction, Schedule management, Interrupt routines, Task scheduling, Performance matric, POSIX, Preemptive scheduler, Sychronization, Embedded Linux internals, OS security Issues, Need of a well tested and debugged RTOS, Case study on VxWorks.  9 Hours.

SLE: Case study of an embedded system for an Adaptive cruise control system in a car.

**Module 5: Device Drivers:**

Introduction, paralleel port device drivers, serial port device drivers, internal programmable timing devices, Interrupt servicing. Context switching deadline and latency, Examples-Initializing an Ethernet Driver, Initializing an RS-232 Driver.  9 Hours.

SLE: Case study of coding for sending application layer byte streams on a TCP/IP network using RTOS VxWorks.

**Text Books:**


**Reference Books:**


**EMBEDDED SYSTEMS LABORATORY**

2. Developing a stand-alone embedded application using VersatilePB and Vexpress and emulation using QEMU.
3. Configuring and compiling U-boot and integrating a standalone application with U-boot.
4. Compiling a custom Linux kernel and running an application under kernel.
5. Configure root file system using busy box.
6. Shell programming
   (a) Round Robin  (b) SJF  (c) FCFS  (d) Priority
8. Implement all file allocation strategies
   (a) Indexed (b) Linked

9. 5. Implement Semaphores
10. Implement all File Organization Techniques.
    (a) Single level directory (b) Two level (c) Hierarchical (d) DAG

11. Implement Bankers Algorithm for Dead Lock Avoidance.
12. Implement an Algorithm for Dead Lock Detection.
13. Implement the all page replacement algorithms
    (a) FIFO (b) LRU (c) LFU

14. Implement Shared memory and IPC.
15. Implement Paging Technique of memory management.
16. Implement Threading (Truly Parallel) & Synchronization Applications.

**Engineering Economics (3:0:0)**

Sub. Code: EC6CO5  
CIE: 50% Marks
Hrs./Week: 3  
SEE: 50% Marks
SEE Hrs: 3 Hrs  
Max. Marks: 100

Course Outcome:

On successful completion of the course, the students will be able to

1. Explain basic concepts of Engineering Economics.
2. Understand concepts of Finance management.
3. Explain Various funding options available to Start-ups.
4. Explain various funding options available for Star-ups
5. Explain how to arrive at Product cost.

**Module 1:**

**Introduction to Engineering Economics:**

6 Hours

SLE: Importance of Economics in Industry,

**Module 2:**

8 Hours

SLE: Gross and Net Domestic Product (GDP and NDP), Gross National Product (GNP)

**Module 3: Finance management:**

Introduction Engineering Finance Management, Roles of a Finance Manager, Brief description on evolution of financial management (Goals, financial decisions in a firm, risk-return trade off), financial statements(Concepts of balance sheets and income statements), Analysis of financial statements.  

10 hours

SLE: Cash Flow Statements, Types of Investment options

**Module 4: Sources of Finance and Funding for Start-ups:**

Sources of finance - Short term, Mid term and long term(shares, debentures, loans, primary and secondary markets Seed Funds, Angle Funds & venture capital), Mergers and acquisitions, Buy outs.  

8 Hours

SLE: Term Sheets, Return On Investment, Internal rate of Return(IRR).

**Module 5: Estimating and Costing:**

Components of costs such as direct material cost, direct labour cost, Fixed, over – heads, factory costs, administrative – over heads, first cost, selling price, calculation of the total cost of various components, Mensuration, estimation of simple components. Break Even Analysis, Concepts of, Depreciation, Methods of Depreciation calculations, Budgets, Replacement and Maintenance analysis – Types of maintenance, types of replacement problem, determination of economic life of an asset.  

8 Hours

SLE: Marginal Cost, Sunk Cost

**Text Books:**


EC6L01 COMMUNICATION NETWORKS LABORATORY (0:0:3) 1.5

LAB 1: Network Administration and Configuration Commands
LAB 2: Packet Sniffing and Wireshark
LAB 3: Understanding of Application-Layer Protocols using Wireshark
LAB 4: Introduction to NS2 and TCL scripting
LAB 5: Simulate a three-node point-to-point network with a duplex link between them for the following cases:
   a. One node act as the sender and receiver and the remaining nodes acts as a repeater
   b. One node act as the sender and two nodes acts receiver and data should flow in two different directions
   c. Two nodes acts as sender and one node acts as receiver. Set queue size to 3 and vary the bandwidth (two cases) and count the packets being dropped

NOTE: Use TCP as transport layer protocol and FTP as traffic source for all cases

Constraint: In all the above cases, no node or link should be kept inactive at any instant of time

LAB 6: To Simulate and study Stop-And-Wait Protocol

LAB 7: Simulate a four-node point-to-point network and connect the link as follows: Apply TCP agent between n0 and n3. Apply relevant applications over TCP and UDP. Change bandwidth and latency (two cases) and determine the number of packets sent by two agents
LAB 8: Simulate a 6 node Ethernet LAN network Change Error rate and Data rate and compare the throughput.

Note: Have two cases of different data and error rates
LAB 9: Understanding the Encoding of Data Packets
LAB 10: Simulation of a Wireless network in NS2.
LAB 11: NETSIM experiments

EC6L02 CMOS VLSI Design Laboratory (0:0:3)1.5

Course outcomes:

At the completion of this course, students will be able to:

1. Use circuit analysis models in analysis of CMOS digital electronics circuits, including logic components and their interconnect.
2. Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
Part A: ASIC Back end design using Cadence tools up to GDSII file generation for simple counters, state machines, adders (min 8 bit) and multipliers (4 bit min).

2. Critical paths and static timing analysis results to be identified. Identify and verify possible conditions under which the blocks will fail to work correctly.

Part B: Analog Design using Virtuoso

1. Design and simulate CMOS Inverter, Verify the functionality, DC response, Generate the layout, LVS and DRC checking, Parasitic extraction and back annotation.
2. Design and Simulate the common source and common drain circuit for the given design parameters, Measure gain, ICMR, and CMRR. Layout generation, LVS and DRC check, parasitic extraction and Back annotation of the circuit designed.
3. Design and simulation of a simple 5 transistor differential amplifier. Measure gain, ICMR, and CMRR. Layout generation, LVS and DRC check, parasitic extraction and Back annotation of the circuit designed.
4. Design and simulation of a two-stage operational amplifier. Measure gain, ICMR, and CMRR. Layout generation, LVS and DRC check, parasitic extraction and Back annotation of the circuit designed.

BIOINFORMATICS (3:0:0)

Sub Code: EC6E101  
CIE: 50% Marks

Hrs./Week: 03  
SEE: 50% Marks

SEE Hrs.: 03  
Max.: 100 Marks

Course Outcomes:

On successful completion of the course the students will be able to:

1. Explain the basics of bioinformatics.
2. Illustrate role of data warehousing and data mining for bioinformatics.
3. Apply various models of bioinformatics.
4. Demonstrate how to deploy the pattern matching and visualization techniques in bioinformatics.
5. Analyse the Microarray technologies for genome expression.

Module 1: Basics of Bioinformatics:
Introduction, Need for Bioinformatics Technologies, Overview of Bioinformatics technologies, Structural Bioinformatics, Data format and processing, secondary resources, Applications, Role of Structural Bioinformatics.  8 Hours.

SLE: Biological Data Integration System.

Module 2: Data Warehousing and Data Mining in Bioinformatics:

Bioinformatics data, Transforming Data to Knowledge, Data Warehousing, Data Warehouse Architecture, data quality, sources of errors, Biomedical Data Analysis, Major Nucleotide Sequence Database, Protein Sequence Database and Gene Expression Database, Software Tools for Bioinformatics Research, DNA data analysis, Central Dogma of Molecular Biology, Phylogenetic Analysis, Protein data analysis, Machine learning, Artificial Neural Network, A neuron model, neural network architecture, Applications in bioinformatics.  8 Hours.

SLE: Machine learning for bioinformatics.

Module 3: Modeling For Bioinformatics:

Hidden Markov modelling for biological data analysis, Sequence identification, Sequence classification, multiple alignment generation, Comparative modelling, Protein Comparative modelling, Comparative genomic modelling, Probabilistic modelling, Bayesian networks, Stochastic Context-Free Grammars, Probabilistic Boolean networks, Molecular modelling, Molecular and Related Visualization Applications, Visualization techniques, Molecular Mechanics.  8 Hours.

SLE: Computer programs for molecular modelling.

Module 4: Pattern Matching and Visualization:

Gene regulation, Promoter Organization, motif recognition, strategies for motif detection, Multi-genes Single Species Approach, Single Gene Multi-species Approach, Multi-genes Multi-species Approach, Visualization, Fractal analysis, What Is a Fractal?, Fractal properties, Fractal dimension, Fractal Analysis, Box counting method, DNA walk models, one dimension, two dimension, higher dimension, Chaos Game representation of Biological sequences; DNA Sequences.  8 Hours.

SLE: Chaos Game Representation of Protein Sequences and Structures, Chaos Game Representation of Amino Acid Sequences Based on the Detailed HP Model.

Module 5: Microarray Analysis:

Microarray technology for genome expression study, schematic flow chart of the cDNA microarray technique, steps involved in a cDNA microarray experiment, image analysis for data extraction, Image preprocessing, segmentation, gridding, spot extraction, Background Correction, Data Normalization, Filtering and Missing Value Estimation, Data Analysis for Pattern Discovery.  8 Hours.

SLE: Cluster analysis, examples of clustering algorithms in the study of gene expression data, hierarchical and partitional clustering, Binary Hierarchical Clustering.
Text Book:


References:

1. NPTEL video lectures on “Biology for Engineers and other non-biologists” by G. K. Suraish Kumar and Madhulika Dixit, Dept. of Biotechnology, IITM.

2. NPTEL video lectures on “Bioinformatics: Algorithms and Applications” by M. Michael Gromiha, Dept. of Biotechnology, IITM.

DIGITAL IMAGE PROCESSING (3:0:0)

Sub. Code: EC6E102  
Hrs./week: 3  
SEE Hrs.: 3  
Max Marks: 100

CIE: 50% Marks  
SEE: 50% Marks

Pre-requisite: Digital Signal Processing (EC5C01)

Course Outcome:

On successful completion of the course, the students will be able to

1. Understand basic principles of digital images, image data structures, and image processing techniques.
2. Understand transform domain of an image and operations in transform domain
3. Understand image processing filtering techniques in both the spatial and frequency (Fourier) domains
4. Understand the processes involved in enhancement and restoration techniques.

Unit 1: Introduction to Image Processing System:

8 Hours.

SLE: Image file formats.

Unit 2: 2D Signals and Systems and Image Transforms:

Introduction, 2D signals, Separable sequence, periodic sequence, 2D systems, classification of 2D systems, 2D construction, 2D Ztransform.

Image Transforms:

8 Hours.

SLE: 2D Digital filter, Wavelet transform.

Unit 4: Image Enhancement:

Introduction, Image Enhancement in spatrate Domain, Enhancement through point operation, Types of point operation. Histogram Manipulation, Linear gray-level transformation, Local or Neighbourhood operation, Median filter, Spatial domain high-pass filtering or image sharpening. Bit-place slicing, image enhancement in the frequency domain, homomorphic filter, Zooming operation, Image arithmetic.  

8 Hours.

SLE: Morphological operations.

Unit 5: Image Restoration


8 Hours.

SLE: Image restoration in satellite images

Unit 6: Image Denoising

Image Denoising, classification of noise in image, median filtering, Trained Average filter, Performance Metrics in Image restoration, Applications of Digital Image Restoration  

8 Hours.

SLE: Image Denoising in medical images.

Text Book:


Reference Book:

Course Outcome:

On successful completion of the course, the students will be able to

2. Explain and implement perceptron, adaline and madaline networks.
3. Understand the basic ideas behind learning algorithms like radial-basis function networks, and SOM.


8 Hours

SLE: Implementation of activation function.


8 Hours

SLE: Brain Maker to Improve Hospital Treatment using Adaline.


8 Hours

SLE: Implementation of Single and Multi layer Neural Networks.

Module 4: Associative Memory and Feedback Networks: Algorithm for pattern association, Hetro and Auto Associative memory Neural Networks, Bidirectional associative memory.

8 Hours


Module 5: CPN and ART: Full Counter Propagation Network, Forward only counter propagation network, ART Fundamentals ART 1, Boltzman Machine, simulated annealing.

8 Hours

SLE: Breast Cancer Detection using ART Networks
Case Study: Improving NN using Hyperparameter tuning, Regularization and batch normalization for application to build a deep neural network model to recognize numbers from 0 to 5 in sign language using TensorFlow.

Text Book:


Reference:


INTERNET OF THINGS (2:0:2)

Sub. Code: EC6E104  CIE:50% Marks
Hrs/week: 2  SEE: 50% Marks
SEE Hrs: 3  Max Marks: 100

Course Outcome:

1. Understand building blocks of Internet of Things, challenges.
2. Describe various protocols for communication.
3. Design and program IoT devices.
4. Explore data analytics and security for IoT.


SLE: IoT Data Management and Compute Stack.


SLE: IEEE 1901.2a, Profiles and Compliances

Module 3: Data and Analytics for IoT, An Introduction to Data Analytics for IoT: Structured Versus Unstructured Data, Data in Motion Versus Data at Rest, IoT Data Analytics Overview, IoT Data Analytics Challenges. Machine Learning: Machine Learning Overview, Supervised Learning, Unsupervised Learning, Neural Networks, 6 hours
SLE: Big Data Analytics Tools and Technology.

Text Books:

Reference Books:
3. Adrian McEwen, “Designing the Internet of Things”, Wiley Publishers, 2013,
4. Daniel Minoli, “Building the Internet of Things with IPv6 and MIPv6”, Wiley

Laboratory
Installing operating systems to Raspberry pi, interfacing sensor and actuators on RPi, collecting sensors data and uploading to open source cloud, Protocols. SCADA.

Agenda 8: Blown up syllabus of 2nd year of UG as per curriculum 2019-20.
- No Change
Agenda 9: Blown up syllabus for 1st year of UG as per curriculum 2020-24.
- No Change
Agenda 10: Scheme & syllabus of all semester of M.Tech courses “Networking and Internet Engineering” as per curriculum 2020-22.
- MOOC Electives and Open Electives are introduced for 3rd semester

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MoM of BoS Meeting held on 13-08-2020

General:

1. MOOC electives and value added electives will be offered for 5th semester.
2. Part of Control system will be done in DSP lab.
3. CMOS VLSI Design and Embedded Systems LTP structure will be swapped.
4. Embedded system laboratory will be replaced with CMOS VLSI Design Laboratory.
5. Advanced Communication course title will be changed as Information and coding theory is also included in same course.
6. Information and coding theory elective in 6th semester will be replaced with new elective Bioinformatics.
7. A new MOOC elective VLSI Verification will be introduced in 5th semester.

Suggestions form BoS members

Dr. B Kanmani:

1. Good to have some non-credit courses like Physical activities.
2. DSP: One type of Filter design thoroughly and remove Chebyshev filter.
3. Control System:
   a. Frame syllabus by referring Gate syllabus and AICTE model.
   b. Focus on Analog and then include Digital.
4. DSP Lab:
   a. Suggested a experiment like by taking audio signal(Music) apply to filter and then get output.
5. Communication and Coding Theory:
   a. Include CRC codes.
   b. In Module – 1 include Polynomials.
   c. Reduce topics in module-5
6. General:
   a. Students should take internship during 1st and 2nd year along with final year.
   b. Credits for Project need to check as per AICTE guidelines.
   c. Frame Curriculum so that in CO_PO mapping PO-4 to PO-11 should also address
Dr. Naveen:
1. **DSP:** Suggested to remove Bilinear transformation and use Lattice space.
2. **Analog and Digital Communication:**
   a. SDR should include in Module-6 and make DPSK and FSK self study.
   b. Text book need to update based on suggestion given during DAB meeting.
3. **Control System:**
   - Include one Module on digital Control system.
4. **DSP Lab:**
   - Suggested a experiment like Impulse response of room then take convulsion.
5. **Communication and Coding Theory:**
   a. LDPC must be include in Module – 4 rather then SLE and can made CRC as SLE.
   b. Advanced word can be replaced with other appropriate word.
   c. Instead of Irregular codes include Polar codes.

Dr. Rudraswamy:
1. **CMOS VLSI Design:**
   a. Add practical exposure for fabrication by industry visit.
   b. Reduce the content in Module-1 and can covered in laboratory.
   c. CMOS theory if discussed in previous semester can be omitted in CMOS VLSI Design.
   d. Testing and verification algorithm can be included in Module-5.