## MEMBERS OF THE BOS MEETING

<table>
<thead>
<tr>
<th>Chairperson</th>
<th>1) Dr. Narasimha Kaulgud, Professor and HOD</th>
</tr>
</thead>
</table>
| Faculty members at different levels covering different specialization. | 2) Dr. S Parameshwara  
3) Dr. C Anjanappa  
4) Dr. Roopa K  
5) Dr. Shashidhara H R  
6) Dr. Rajalekshmi Kishore |
| Members | 1) Raghupathi S, Tech. Leader, CISCO Systems Bengaluru |
| Two experts in the subject from outside the College. | 2) Dr. Rudraswamy, Professor, Dept. of ECE, SJCE, Mysuru |
| Members | 3) Dr. B Kanmani, Prof, and Head, Dept of Telecommunication, MS college of Engg., Bengaluru. |
| One expert from outside the College, to be nominated by the Vice Chancellor, VTU, Belgaum | 4) Dr. Sujatha Jaganath, Wipro, Bangalore |
| Member | 5) Dr. Naveen, Professor, Dept. of Electrical Engineering IIT, Dharwad. |
| One representative from industry / corporate sector / allied area relating to placement. | Membe |
| Member |  |
| One postgraduate meritorious alumnus, to be nominated by the Principal. | Membe |
| Member |  |
DEPARTMENT OF E&C

BOS MEETING

AGENDA

1. Suggestions from DIAB, DAAB board.

2. Blown up syllabus of 4th year of UG as per curriculum 2018-19

3. Any other academic matters.
**Agenda 1:** Suggestions from DIAB, DAAB board.

**Suggestions from DIAB members**

1. More emphasis on coding and algorithm.
2. Invited talks on advance topic from alumni network.
3. Encourage student participations in online hackathons to improve coding knowledge.
4. Pattern Recognition and Machine learning
   a. Include more e-link and resources for references.
   b. Split the module in more generic content like Dimensionality reduction, supervised learning, unsupervised learning and DNN.
   c. Reduce advance concepts in module 4 and 5.

**Suggestions from DAAB members**

1. Add laboratory component specially coding part in ANN.
2. Formation of committee for long term vision towards student driven activity.
3. Include Gate/ above L3 questions for CIE/SEE.
4. Include advance technologies in communication related courses but not specific like 4G, LTE and 5G etc.
5. Increasing the level of difficulty during laboratory examination.
6. System Verilog
   a. Do laboratory session is also part of this this course?
   b. In Unit – 5, SLE component of unit 4 that is “synthesis guidelines for interface method” should be included.
7. Reconfigurable Computing
   a. Discussion with respect to SOPC.
**Agenda 2:** Blown up syllabus of 4th year of UG as per curriculum 2018-19

1. In 8th semester all members suggested to have one stream of electives for students.
2. Since 7th semester has Mixed Mode VLSI design laboratory, swap wireless communication as elective and Mixed Signal design as Core course.
3. Advance Signal Processing of 8th semester course is renamed as “Signal processing and machine learning”
4. BoS members approved following new electives for 7th semester:
   a. System Verilog.
   c. FPGA based Embedded Systems. (open Elective)
5. BoS members approved following new electives for 8th semester:
   a. Reconfigurable computing.

The following blown-up Syllabus for 4th year was approved for students admitted in academic year 2018-22.

**Scheme for IV Year**

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>Category</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>Cr</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EC7C01</td>
<td>Antenna and Microwave</td>
<td>Department core</td>
<td>3</td>
<td>2</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>EC7C0X</td>
<td>Mixed Signal design</td>
<td>Department core</td>
<td>3</td>
<td>2</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>EC7E2X</td>
<td>Department Elective - 2</td>
<td>Department Elective</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>EC7E3X</td>
<td>Department Elective - 3</td>
<td>Department Elective</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>EC7IXX</td>
<td>Industry driven Elective</td>
<td>Industry driven Elective</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>EC7OXX</td>
<td>Open Elective</td>
<td>Open Elective</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>7</td>
<td>EC7L01</td>
<td>Mixed mode VLSI design Laboratory</td>
<td>Laboratory</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>EC7L02</td>
<td>Advanced Communication Laboratory</td>
<td>Laboratory</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>EC7C03</td>
<td>Seminar/ paper presentation</td>
<td>Seminar</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>EC7C04</td>
<td>Project Phase - 1</td>
<td>Project</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Course Code</td>
<td>Course Title</td>
<td>Department Elective (Elective - 2)</td>
<td>Dept Elective (Elective - 3)</td>
<td>Industry driven Elective</td>
<td>Open Elective</td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>-------------</td>
<td>-----------------------------------------------</td>
<td>-----------------------------------</td>
<td>-------------------------------</td>
<td>-------------------------</td>
<td>--------------</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>EC7E201</td>
<td>Optical Communication System</td>
<td>3 0 0 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>EC7E202</td>
<td>Multimedia Communication</td>
<td>3 0 0 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>EC7E203</td>
<td>Network Security</td>
<td>3 0 0 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>EC7E30X</td>
<td>Wireless Communications</td>
<td>3 0 0 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>EC7E302</td>
<td>RF Electronics</td>
<td>3 0 0 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>EC7E30X</td>
<td>System Verilog</td>
<td>3 0 0 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>EC7EXX</td>
<td>Pattern Recognition and Machine Learning</td>
<td>3 0 0 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>EC7I01</td>
<td>IDE</td>
<td>2 0 0 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>EC7O01</td>
<td>Internet of Things</td>
<td>2 0 0 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>EC7O0x</td>
<td>FPGA based Embedded Systems</td>
<td>2 0 0 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Total Credits:** 23  
**Total Contact Hrs:** 26
<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Subject Code</th>
<th>Subject Category</th>
<th>Subject</th>
<th>Category</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>Cr.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EC8E4X</td>
<td>Department Elective - 4</td>
<td>Department Elective</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>EC8E5X</td>
<td>Department Elective - 5</td>
<td>Department Elective</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>EC8E6X</td>
<td>Department Elective - 6</td>
<td>Department Elective</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>EC8C01</td>
<td>Internship</td>
<td>Internship</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>EC8C02</td>
<td>Major Project</td>
<td>Major Project</td>
<td>0</td>
<td>0</td>
<td>8</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Total Credits</strong></td>
<td></td>
<td></td>
<td></td>
<td>16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Total Contact Hrs.</strong></td>
<td></td>
<td></td>
<td></td>
<td>17</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Previous elective groups</th>
<th>Modified elective groups</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1 EC8E401 Artificial Intelligence</td>
<td>Artificial Intelligence</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>2 EC8E402 Speech Processing</td>
<td>Satellite Communication</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>3 EC8E403 Signal Processing and Machine Learning</td>
<td>Low Power VLSI</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>4 EC8E501 Satellite Communication</td>
<td>Speech Processing</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>5 EC8E502 Mobile Computing</td>
<td>Mobile Computing</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>6 EC8E503 Wireless Networks</td>
<td>Automotive Electronics</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>7 EC8E601 Low Power VLSI</td>
<td>Signal Processing and Machine Learning</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>8 EC8E602 Automotive Electronics</td>
<td>Wireless Networks</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>9 EC8E603 Nano Electronics</td>
<td>Nano Electronics</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>10 EC860X Reconfigurable Computing</td>
<td>Reconfigurable Computing</td>
<td>3</td>
<td>0</td>
</tr>
</tbody>
</table>

* Course integrated with Laboratory
ANTENNA AND MICROWAVE  (3:2:0)

Sub. Code: EC7C01                  CIE: 50 Marks
Hrs./Week: 3                      SEE: 50 Marks
SEE Hrs: 3 Hrs.                  Max. Marks: 100

Prerequisite: Electromagnetic Field Theory (EC4C04)

Course Outcome:
On successful completion of the course students will be able to:

1. Design an antenna/array for given specification.
2. Discuss the types of transmission lines and analyze mode of propagation through them
3. Apply microwave network theory to analyze the operation of microwave components and devices
4. Discuss the various sources of noise in microwave circuits
5. Discuss the basic principles of operation of RADAR systems

Unit 1: Antennas
SLE: Planar array, Circular array, Three-dimensional characteristics, Simulation of Dipole Antenna.

Unit 2: Transmission Lines

Unit 3: Microwave network Theory and Passive Devices
Microwave Network Analysis, Basics of Impedance and Admittance Matrices, The Scattering Matrix, Reciprocal Networks and Lossless Networks, A Shift in Reference Planes, Generalized Scattering Parameters, The transmission (ABCD) matrix, ABCD matrix to/from S-Matrix, Passive Devices---Three-Port Networks (Circulators), Four-Port Networks 10 Hrs
SLE: Two-Port Networks (Isolators), Directional couplers, Simulating and plotting S parameters for Circulator, Isolator and Magic Tee.
Unit 4: Noise in Microwave Circuits
Noise in Microwave Circuits, Dynamic Range and Sources of Noise, Noise Power and Equivalent Noise Temperature, Measurement of Noise Temperature, Noise Figure, Definition of noise figure, Noise Figure of a Cascaded System.  
SLE: Noise Figure of a Passive Two-Port Network and related numericals

Unit 5: An Introduction to Radar
Basic Radar, The simple form of the Radar equation, Radar transmitter and receiver block diagram, Radar frequencies, applications of Radar, Pulse Repetition Frequency (PRF), Introduction to Doppler and MTI Radar.  
SLE: Delay line Cancellers, Staggered PRF, Simulation of Doppler Radar.

Text Books:

Reference Book:

MIXED SIGNAL DESIGN(3:2:0)

Course Code: EC7C0x  
Hrs./Week : 3 Hrs  
SEE Hrs.: 3  
Max. Marks : 100

Prerequisite: Analog CMOS IC 1 & 2

Course Outcome:
On successful completion of the course, the students will be able to,
1. Design the building blocks of data conversion systems.  
2. Understand the non-idealities of data converters.  
3. Design digital to analog converters and analog to digital converters.  
4. Identify the characteristics and quantify the performance of data converters.

Module 1: Building Blocks of Data Conversion Systems – 1  
SLE: Switched capacitor Comparators.

Module 2: Building Blocks of Data Conversion Systems – 2  
Amplifiers: Two-stage Amplifier Design, Frequency compensation, Biasing circuits: Supply-Independent Biasing, Bandgap References, Constant Gm Biasing  
SLE: Folded Cascode Amplifier.

Module 3: Digital to Analog Converters (DACs)
Module 4: Analog to Digital Converters (ADCs) 8Hrs.
Fundamentals: Non-Idealities and Performance Metrics, ADC Architectures: Flash ADC, Nyquist Rate ADC, Oversampling ADC (DSM), Pipeline ADC, Review of state-of-the-art Architectures.
SLE: Integrating ADCs, SAR ADC.

Module 5: Precision Techniques, Testing and Characterization 8Hrs.
SLE: Calibration Techniques, Code Density Test

Text Books:

References:

OPTICAL FIBER COMMUNICATION (3:0:0)

Sub. Code: EC7E201 CIE: 50% Marks
Hrs/week: 3 SEE: 50% Marks
SEE Hrs: 3 Max Marks: 100

Course Outcome:
On successful completion of the course, the students will be able to
1. Identify the basic elements of optical fiber transmission link, fiber modes configurations and structures.
2. Analyze the different kind of losses, signal distortion in optical wave guides and their signal degradation factors and the various optical source materials, LED structures, Laser diodes. Principles of Photo diodes.
3. Apply the fiber optical receivers concepts in communication, basics of optical amplifiers, receiver operation and configuration.
4. Analyze the fiber optical networks like SONET/SDH and Operational principles of WDM.

Module 01: Overview of optical fiber communication:
Key elements of optical fiber systems, Advantages and Disadvantages of optical fiber Communication, Basic optical laws and definitions, optical fiber modes and configuration, Mode theory of circular wave guides: Overview, summery of key modal concepts, single mode
fibers, graded index fibers, fiber materials.

**SLE:** Fiber fabrication.

**Module 02: Signal Degradation in Optical Fibers:**
Attenuation, signal losses in optical wave guides: Absorption, Scattering losses, Bending losses. Signal distortion in Fibers.

**SLE:** Characteristics of single mode fibres.

**Module 03: Optical Sources and Detectors:**
Introduction, LED’s, LASER diodes: LASER diodes Modes and threshold conditions, single mode Lasers, Principles of Photo diodes.

**SLE:** Photo detector noise.

**Module 04: Optical Receiver and Digital Transmission System:**
Fundamental receiver operation: Digital signal transmission, error sources, receiver configurations. Overview of analog links

**SLE:** Burst mode receivers.

**Module 05: Optical Amplifiers and Optical Networks**
Basic applications and types of optical amplifiers, semiconductor optical amplifiers, Erbium doped fiber amplifiers. SONET / SDH. Operational principles of WDM.

**SLE:** Nonlinear effects on network performance.

**Text Book:**

**Reference Book:**

**MULTIMEDIA COMMUNICATION (3:0:0)**

**Sub. Code:** EC7EXXX  
**CIE:** 50% Marks  
**Hrs./week:** 3  
**SEE:** 50% Marks  
**SEE Hrs.:** 3  
**Max Marks:** 100

**Course Outcomes:**
On successful completion of the course the students will be able to:
1. Identify various Multimedia Communication Models.
2. Apply compression methods and standards for Multimedia communication.
3. Apply compression methods and standards for video signals.
4. Analyse synchronisation issues in multimedia communication.

**Module 1: Introduction to Multimedia:**

[Signature]
Introduction to multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology, network QoS and application QoS, Text, images, audio and video.

**SLE:** Digitization principles. 8 Hrs.

**Module 2: Text and Image Compressions:**
Text and image compression, compression principles, text compression- modified Huffman, LZW, Embedded zerotree wavelet (EZW), Document Image compression using T2 and T3 coding, image compression- GIF, TIFF and JPEG. SLE: Runlength and Huffman coding. 8 Hrs.

**Module 3: Audio and Video Compressions:**
Audio and video compression, audio compression - principles, DPCM, ADPCM, Adaptive and Linear predictive coding, Code-Excited LPC, Perceptual coding, MPEG and video compression, video compression principles. SLE: Dolby coders. 8 Hrs.

**Module 4: Video Compression Standards:**
H.261, H.263, MPEG, MPEG 1, MPEG 2, MPEG-4 and Reversible VLCs, MPEG 7, standardization process of multimedia content description, MPEG 21 multimedia framework. SLE: MPEG 2000 compression technique. 8 Hrs.

**Module 5: Synchronization:**
Notion of synchronization, presentation requirements, reference model for synchronization, Introduction to SMIL, Multimedia operating systems, Resource management, and process management techniques. SLE: Case Studies like MHEG, HyTime. 8 Hrs.

**Text Books:**

**Reference Books:**

**NETWORK SECURITY (3:0:0)**

<table>
<thead>
<tr>
<th>Sub Code: EC7E203</th>
<th>CIE: 50% Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Credits: 3</td>
<td>SEE: 50% Marks</td>
</tr>
<tr>
<td>Hrs./week: 3</td>
<td>Max Marks: 100 Marks</td>
</tr>
</tbody>
</table>

**Course Outcome:** On successful completion of the course, the students will be able to:
1. Apply the symmetric key crypto systems.
2. Apply the concepts of public key encryption techniques and explain applications of hash functions.
3. Explain Digital Signatures along with Web and IP security.
4. Explain Firewall and Cloud security concepts.

Module 1: Introduction to Network Security and Symmetric Ciphers:
Need for network security, Services, mechanisms and attacks, Model of symmetric cryptosystem, Cryptanalysis and Brute-Force Attack, Substitution Techniques: Caesar Cipher, additive cipher, Multiplicative Ciphers, Affine Ciphers, Monoalphabetic Cipher, Frequency/Statistical analysis, Homophones, Playfair Cipher, Hill Cipher; involving both 2x2 and 3x3 matrices, Polyalphabetic Cipher, Vigenère Cipher, Autokey Cipher, Vernam Cipher, One Time Pad.

Hrs: 8
SLE: Single and Double transposition ciphers, Steganography, Privacy preservation techniques.

Module 2: Block Cipher and Encryption Standards:

Hrs: 10
SLE: Block cipher design principles; Number of rounds, design of function F; strict avalanche criterion (SAC), bit independence criterion (BIC), S-BOX Design, guaranteed avalanche (GA) criterion, Key Schedule Algorithm.

Module 3: Public-Key Encryption and Hash Functions:
Principles and applications of public-key cryptosystems, requirements for public-key cryptosystems, One-way function, Trap-door one-way function, public-key cryptanalysis, brute-force attack, Probable-message attack. Rivest-Shamir-Adleman (RSA) algorithm, description of the algorithm, computational aspects, security of RSA. Other Public-Key Cryptosystems; Diffie-Hellman key exchange algorithm, discrete logarithm, Key exchange protocol, man in the middle attack, Elliptic Curve Cryptography (ECC), security of Elliptic curve cryptography, Applications of Cryptographic Hash Functions.

Hrs: 8
SLE: Applications of Message Authentication Functions.

Module 4: Digital Signatures, Web and IP Security:

Hrs: 8

Module 5: Firewalls and Cloud security:
Architecture, cloud security risks and countermeasures, data protection in the cloud, An Encryption Scheme for a Cloud-Based Database, cloud security as a service. **Hrs: 6**

**SLE:** Firewall configurations, Intruders; classes of intruders, Intrusion detection techniques; Statistical anomaly detection, Rule-based detection.

Textbook:


Reference Books:


**System Verilog(3:0:0)**

<table>
<thead>
<tr>
<th>Sub Code: EC7E30X</th>
<th>CIE: 50% Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hrs./Week: 03 Hrs</td>
<td>SEE: 50% Marks</td>
</tr>
<tr>
<td>SEE Hrs.: 03</td>
<td>Max.: 100 Marks</td>
</tr>
</tbody>
</table>

**Course Outcomes:**
On successful completion of the course the students will be able to:
1. Apply object oriented techniques for digital system verification.
2. Develop the System Verilog codes for digital system design and verification.
3. Create/build test benches for the basic design/methodology.
4. Construct the constrained random tests for verification of the functional coverage.
5. Design and build the ATM as an example.

**Case study: Design a synchronous and asynchronous counters**

**Module 1: Verification Guidelines:**
The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components.

**Data Types:**
Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with type def, creating user defined structures, type conversion, Enumerated types, constants and strings, Expression width.

**Hrs**

**SLE:** Net Types

**Module 2: Procedural Statements and Routines:**
Converting the test bench and design:
Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.  
8 Hrs
SLE: Local data storage and Connecting It All Together and Program – Module Interactions

Module 3: Randomization:
8 Hrs
SLE: Random Generators and Random Device Configuration

Module 4: Threads and Interprocess Communication and coverage Types:
Working with threads, Disabling threads, Interprocess communication, Events, semaphores, Mailboxes, Building a test bench with threads and Interprocess Communication, Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Coverage options,  
8 Hrs
SLE: Verification with interfaces

Module 5: Synthesis and A complete Design Modeled with SV:
Synthesis guidelines for interface methods, SV ATM example, Data abstraction, Interface encapsulation, Design top level, Receivers and transmitters, Testbench.  
7 Hrs
SLE: Analyzing coverage data, measuring coverage statistics during simulation

Text Book:
3. Stuart Sutherland, “RTL modeling with System Verilog for simulation and synthesis: using System Verilog for ASIC and FPGA design” Tualatin, 2017

RF ELECTRONICS (3:0:0)

Sub Code: EC7E302  CIE: 50% Marks
Hrs./Week: 03 Hrs  SEE: 50% Marks
SEE Hrs.: 03  Max.: 100 Marks

Course Outcome:
On successful completion of the course, the students will be able to:

1. Calculate radio, microwave and link power and noise budgets.
2. Design and Analyze LNA topologies, switching and non-linearity behaviour of the system.
3. Understand the various types of RF mixers
4. Illustrate the characteristics of PLL and Synthesizers.
5. Interpret and Deploy different RF transceiver architectures.


Module 2: LOW-NOISE AMPLIFIERS: General Considerations: Problem of Input Matching, LNA Topologies, Gain Switching, Band Switching, High-IP2 LNAs, Nonlinearity Calculations.

Module 3: MIXERS: General Considerations, Passive and active Down conversion Mixers, Improved Mixer Topologies, Upconversion Mixers.

Module 4: PHASE-LOCKED LOOPS and Synthesizers: Basic Concepts, Type-I PLLs, Type-II PLLs, Design Procedures.

Module 5: TRANSCIEVER ARCHITECTURES: General Considerations, Receiver Architectures: Basic and Modern Hetrodyne reciever, Transmitter Architectures: Direct and Hetrodyne Transmitters.

Text Books:

Reference Books:
2. For Design Examples:  

WIRELESS COMMUNICATIONS - EC7E30X (3:0:0)

Sub. Code: EC7E30X  CIE: 50% Marks
Hrs. /Week: 3  SEE: 50% Marks
SEE Hrs: 3 Hrs.  Max. Marks: 100

Course Outcome:

On successful completion of the course, the students will be able to:

1. Review and classify the different generations of wireless cellular communication systems and fading concepts.
2. Apply and study the cellular communication concepts.
3. Apply and examine the multiple antennas systems using symbolic representations
4. Research on Multicarrier modulation (OFDM) and its implementation
5. Examine the LTE architecture and its channel specifications

Module 1: Evolution of Mobile Radio Communication and Fading Concepts:
Evolution and Deployment of cellular Telephone systems: Different generations of wireless cellular networks, 1G cellular systems, 2G cellular systems, 2.5G cellular systems, 3G cellular systems, 4G cellular systems and beyond, wireless standard organizations, fading: Delay Spread and Coherence Bandwidth, Doppler Spread and Coherence Time, Angular Spread and Coherence Distance

8Hrs
SLE: LTE Advanced and 5G cellular systems

Module 2: Mobile Communication Concepts
Introduction, Concept of cellular communications, Cell Fundamentals, Frequency Reuse concepts, Concept of cell cluster, Cellular layout for frequency reuse, Geometry of hexagonal cell, Frequency Reuse Ratio, Co-channel and Adjacent Channel Interference, Various mechanism for capacity increase, Cell Splitting, Sectoring, Microcell Zone Concept, Channel Assignment Strategies, Handoff Strategies.

8Hrs
SLE: Concepts of femto, Pico, micro, macro cells and umbrella cell approach

Module 3: Multiple Antennas
Narrowband MIMO Model, Parallel Decomposition of the MIMO Channel, MIMO Channel Capacity, MIMO Diversity Gain: Beamforming, Diversity-Multiplexing Trade-offs, Frequency-Selective MIMO Channels, Smart Antennas

8Hrs  SLE: Space-Time Modulation and Coding, Cooperative MIMO

Module 4: Multicarrier Modulation
Data Transmission using Multiple Carriers, Multicarrier Modulation with Overlapping Subchannels, Mitigation of Subcarrier Fading, Discrete Implementation of Multicarrier
Modulation, Challenges in Multicarrier Systems

8Hrs  SLE: OFDMA, SC-FDMA, NOMA

Module 5: Overview and Channel Structure of LTE

8Hrs.
SLE: DL and UL Transport channel processing overview

Text Books:

Reference books:

INTERNET OF THINGS (2:0:0)

Sub. Code:    EC7O01         CIE: 50% Marks
Hrs/week:    2               SEE: 50% Marks
SEE Hrs:     2               Max Marks: 50

Course Outcome:

On successful completion of the course, the students will be able to

1. Explain the application, challenges and architecture of IoT.
2. Use sensors and actuators with Controllers
3. Investigate various protocols and wireless technologies.

Module 1: Introduction to Internet of Things


7 Hrs

SLE: M2M

Module 2: Sensors, actuators and IoT Protocols
Parameters for selection of sensors, Proximity sensor, photoelectric sensor, temperature sensor, position sensor, pressure sensor, smart sensor, Linear actuator, circular actuator, Controllers. Application Protocols – MQTT, REST/HTTP, LORa, CoAP, XMPP, Infrastructure Protocols - Wi-Fi, Bluetooth, Zigbee, RFID.

9 Hrs
SLE: BLE, Z-Wave

7 Hrs

SLE: IOT in healthcare

Text Books:

3. Daniel Minoli, “Building the Internet of Things with IPv6 and MIPv6”, Wiley Publisher.

Reference Books:

1. Adrian McEwen, “Designing the Internet of Things”, Wiley Publishers, 2013,
2. Arshdeep Bhaga and Vijay Madisetti “Big Data Science & Analytics”.

FPGA based Embedded Systems (2:0:0)

Sub Code: EC7O0X                CIE: 50% Marks
Hrs./Week: 02                    SEE: 50% Marks
SEE Hrs.: 02                     Max.: 100 Marks

Course Outcomes:
On successful completion of the course the students will be able to:
1. Summarize on Digital system design.
2. Understanding the concept of programming an embedded system.
3. Identify FPGA architecture, interconnect and technologies.
4. Recognize different FPGAs and implementation methodologies.

Module 1: Revision of Digital systems:

Digital system design options and tradeoffs, Number System, Boolean Algebra, Demorgan’s Theorem, Logic Gates, SOP and POS forms, MVP techniques, Combinational circuits: Adders, Mux & Demux, Sequential design: Latches, Flip-Flops, Counters (Synchronous and Asynchronous), state machine design: FSM, Different kinds of programmable logic devices: Field Programmable Gate Array (FPGA), Programmable Logic Device (PLD), FPGA applications. Adjoining devices. Instruments and software. 8 Hrs

SLE: Encoders and Decoders

Module 2: Programming of Embedded systems:

SLE: Lint, Version Control.

**Module 3: FPGA Configuration:**


**Overview of FPGA architectures and technologies:** FPGA Architectural options, granularity of function and wiring resources, coarse V/s fine grained, Logic block architecture: FPGA logic cells, timing models, power dissipation I/O block architecture: Input and Output cell characteristics, clock input, Timing, Power dissipation, Programmable interconnect - Partitioning and Placement, Routing resources, delays; Applications-Embedded system design using FPGAs. **10 hrs**

SLE: DSP using FPGAs, Dynamic architecture using FPGAs.

**Lab Components:** Simulation/implementation exercises of combinational, sequential circuits on Xilinx/Altera boards.

**Text Books:**


**Reference Books:**


**Pattern Recognition and Machine Learning (3:0:0)**

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<th>Sub. Code: EC7EXXX</th>
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<td>Hrs./week: 3</td>
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**Course Outcome:**

On successful completion of the course, the students will be able to:
1. Extract features for Pattern recognition.

2. Analyze the Parameter Estimation techniques.

3. Apply neural network models for pattern recognition.

4. Analyse the deep learning concepts.

**Module 1: Introduction to Pattern Recognition:**
Overview of: Pattern Recognition, Artificial Neural Network and Machine Learning. Feature Extraction, Bayes Decision Theory, Binary Features.
8Hrs.
SLE: Normal Density and Discriminant Function.

**Module 2: Parameter Estimation:**
Maximum Likelihood Estimation, Probability Density Estimation, Dimensionality Problem, Multiple Discriminant Analysis, Principal Component Analysis. 8Hrs.
SLE: Affine transformation.

**Module 3: Perceptron and Multi Layer Neural Networks:**
Perceptron Criteria, Relaxation Criteria, Minimum Squared Error (MSE) Criteria, Neural Networks for Pattern Recognition. 8Hrs.
SLE: Hopfield Network.

**Module 4: Models for Representation, classification and Clustering:**
Support Vector Machine, Clustering, Clustering using minimal spanning tree, SOM, Autoencoder, Autoencoder Vs. PCA, Autoencoder applications. 8Hrs.
SLE: Temporal Pattern recognition.

**Module 5: Deep learning:**
Introduction to Deep Learning, Deep Neural Network and approaches, Convolution, Cross Correlation, CNN Architecture, MLP versus CNN, AlexNet, Deconvolution Layer, Semantic Segmentation, loss function, Image Denoising. 8Hrs.
SLE: Generative Adversarial Network.

**Note:** Tutorial/ Exercise/ Handson using software tools as provided by the course instructor will be part of the course, CIE and SEE.

**Text Books:**

**Reference Books:**

Artificial Intelligence
Course Outcomes:

On successful completion of the course the students will be able to:

1. Justify the need of Artificial Intelligence in problem solving.
2. Analyze different search techniques, Rules and Rule-based systems,
3. Solve Constraint Satisfaction Problems and Machine Gaming Systems
4. Identify the different ways of Solving Decision systems in Supervised Learning.
5. Classify and Identify data in Unsupervised Learning.

Note: YouTube Links are proposed at the time of preparing the Syllabus and might change.

MODULE 1: Intro to Artificial Intelligence - 08 Hours


MODULE 2: Searches and Rule Based Systems (CO2) - 08 Hours
Basic Search, Optimal Search – British Museum, Depth First, Breadth First, Hill Climbing and Beam, Branch & Bound and A* Algorithm. Rule and Rule Chaining – Rule-Based deduction systems, Procedures for Forward and Backward chaining, Best First Search

Self Learning Exercise: Deep Sequence Modelling (https://www.youtube.com/watch?v=SEnXr6v2ifU)

MODULE 3: Trees, Adversarial Search and CSP and Learning by Machines – 08 hours (CO2)
Genetic Algorithm (Optimization), MINMAX Gaming, Alpha-Beta Pruning, Constraint Satisfaction Problems, Introduction, Nearest Neighbours (kNN), Numeric constraints (Crypto Arithmetic)


MODULE 4: Machine Learning – Supervised Learning (CO3) – 08 Hours
Learning through: Identification Trees and Disorders, Linear Classification, Classifying using : Naïve Bayes ,Logistic Regression, Linear Regression, Support Vector Machines

Self Learning Exercise: Deep Generative Modelling (https://www.youtube.com/watch?v=rZufA635dq4)

MODULE 5: Neural Nets (CO4) – 08 Hours
Training by Neural Nets, Deep Neural Nets, Back Propagation in NN, Convolution Neural Network (CNN), Grouping un-labelled items using k-means clustering Deep
Self Learning Exercise: Reinforcement Learning (https://tinyurl.com/54tru7nc)

TEXT BOOK:
1. Artificial Intelligence – A Modern approach, (3e) Stuart Russel and Peter Norvig - Pearson

Reference Books:
1. Decision Support and Business Intelligence System (9e), PEARSON Efraim Turban and et. al.

SPEECH PROCESSING (3:0:0)

Sub. Code: EC8EXXX  CIE: 50% Marks
Hrs./week: 3  SEE: 50% Marks
SEE Hrs.: 3  Max Marks: 100

Course Outcome:
On successful completion of the course, the students will be able to:
1. Analyze the basic concepts of speech processing and mathematical foundations needed for speech processing.
2. Process and visualize speech signals.
3. Apply predictive technique for speech compression.
4. Apply the concepts and algorithms of speech processing for speech and speaker recognition.

Module 1: Basic Concepts:
Process of speech production, Time Domain Models for Speech Processing: Time dependent processing of speech, Short time energy and average magnitude, Speech vs silence discrimination using energy & zero crossings, Sampling speech signals. 8 Hrs.

SLE: Pitch period estimation and Median smoothing, Adaptive quantization, Differential quantization.

Module 2: Short Time Fourier analysis:
Fourier Transform Interpretation, Linear Filtering interpretation, Filter bank summation method, overlap-add method, Design of digital filter banks, Implementation using FFT, Spectrographic displays. 8 Hrs.

SLE: Analysis synthesis systems.

Module 3: LPC and Speech Enhancement:
Basic principles of linear predictive analysis, Pitch Detection using LPC parameters, Formant Analysis using LPC parameters, LPC Vocoder, Voice Excited LPC vocoder. Speech


Module 5: Automatic Speech Recognition: Introduction to Automatic Speech Recognition, Speech recognition vs. Speaker recognition, Signal processing and analysis methods, Hidden Markov Models, Artificial Neural Networks. SLE: Pattern comparison techniques. 8 Hrs.

Note: Practical assignments as provided by the course instructor will be part of the course.

Text Books:

Reference Books:

SIGNAL PROCESSING and MACHINE LEARNING (3:0:0)

Subject code: EC8E403  CIE: 50% Marks
Hrs./week: 3  SEE: 50% Marks
SEE Hrs: 3  Max Marks: 100

Course Outcome:
On successful completion of the course, the students will be able to:
1. Convert a sampled signal to a different sampling rate.
2. Design an adaptive filter.
3. Estimate spectral characteristics of signals.
4. Explain the use of Wavelets and multiresolution.
5. Apply ML algorithm for signal processing.

Module-1 Multirate signal processing:
Review of sampling, Nyquist rate, aliasing, reconstruction, anti-aliasing filters. Decimation and interpolation, Sampling rate conversion and implementation, Digital filter banks, Sampling rate conversion for multistage and bandpass signals. 8 Hrs.
SLE: Applications of multirate signal processing, Implementation of sampling rate conversion.

**Module-2 Adaptive filters:**
Adaptive filter applications – System identification, Adaptive channel equalization, Echo cancellation, Adaptive line enhancer, Adaptive noise cancellation, LPC of speech signals, LMS and RLS algorithms. 8Hrs.

SLE: Echo cancellation, k-means clustering, LMS using matlab

**Module-3 Power spectral estimation:**
Estimation of power spectra, Non-parametric estimation – Barlet, Welch methods, characteristics of nonparametric power spectrum estimators, parametric power spectrum estimation – Auto correlation model parameters, Yule-walker method, unconstrained least squares, AR model parameters. 8Hrs.

SLE: Selection of AR model, MA and ARMA models

**Module -4 Wavelets:**
Continuous time wavelets, CWT as operator, inverse CWT, DWT and vector subspaces, MRA, Formal definition, scaling functions and subspaces Wavelet basis for MRA. 8Hrs.

SLE: CWT as correlation, Direct sum decomposition of MRA.

**Module -5 Machine learning for Signal processing:**
Supervised learning, Classification models to predict class models, regression models, classifying iris species. 8Hrs.

SLE: Representing data and features.

**Text Books:**

**Reference Books/Links:**
5. NPTEL Course: https://www.youtube.com/watch?v=HVGW85eGPQQ&list=PLyqSpQzTE6M_h5UgZWpybzBVDGmHghQ6
7. https://www.sp4comm.org/
Course Outcome:
On successful completion of the course, the students will be able to:

1. Inspect the fundamentals of satellite communication.
2. Categorize the several noises and apply signal loss factors in satellite communication.
3. Apply Kepler laws and examine various satellite terminologies.
4. Distinguish between the working of earth segment and space segment of satellite communication.
5. Examine the various satellite services.

Module 1: FUNDAMENTALS OF SATELLITE AND PROPAGATION IMPAIRMENTS

Introduction, frequency allocation, INTELSAT, Indian Satellite systems.
Propagation impairment: Introduction, atmospheric loss, ionosphere effects, rain attenuation, other propagation impairments.

9Hrs.

SLE: Tropospheric Impairments, noise and multipath interference.

Module 2: ORBITS

Introduction, Kepler laws, definitions, orbital element, apogee and perigee heights, orbit perturbations, inclined orbits, calendars, universal time, sidereal time, orbital plane and sun synchronous orbits.

9Hrs.

SLE: launching vehicles, polar orbits, poloar orbiting satellite.

Module 3: SPACE SEGMENT and SPACE LINK

Introduction, power supply units, altitude control, station keeping, thermal control, TT&C Subsystem, transponders, antenna subsystem.
SPACE LINK: Introduction, EIRP, transmission losses, link power budget Equation, system noise, CNR, uplink and downlink, combined CNR.

9Hrs.

SLE: Combined CNR, Equipment reliability and space qualification.

Module 4: Earth Segment

Introduction, receive only home TV system, outdoor unit, indoor unit, MATV, CATV, Tx–Rx earth station.
8Hrs.
SLE: Hybrid Satellite Terrestrial Network (HSTN), Satellite communication in 5G Mobile services.

**Module 5: DBS, SATELLITE MOBILE AND SPECIALIZED SERVICES**
Introduction, orbital spacing, power ratio, frequency and polarization, transponder capacity, bit rates for digital TV, satellite mobile services, VSAT, RadarSat. GPS: Introduction, GPS position and location principles, GPS receiver and codes, Orbcomm.

8Hrs.
SLE: Iridium, Satellite Navigation Systems

**Text Books:**

**Reference books:**

**MOBILE COMPUTING (3:0:0)**

**Sub. Code:** EC08E502  
**Hrs./week:** 3  
**SEE Hrs:** 3  
**CIE: 50% Marks**  
**SEE: 50% Marks**  
**Max Marks:** 100

**Course Outcome:**
On successful completion of the course, the students will be able to:
CO1: Explain components of wireless communication.
CO2: Compare and contrast different techniques in mobile communication like ????
CO3: Explain the Workflow of Mobile OS
CO4: Illustrate various Markup Languages for mobile computing
CO5: Program Mobile Apps using architecture like J2ME.

**Module 1: Mobile Computing Architecture**

**SLE:** SMMO, SMS as Information bearer, Introduction to Java, Bytecode

**8 Hrs.**

**Module 2: GPRS and Packet Data Network**
GPRS Network Architecture, GPRS Network Operations, Data Services in GPRS, Applications for GPRS, Billing and Charging in GPRS. Spread Spectrum technology, IS-95,
CDMA versus GSM, Wireless Data, Third Generation Networks, Applications on 3G, Mobile Client: Moving beyond desktop, Mobile handset overview, Mobile phones and their features, PDA.

**SLE:** Design Constraints in applications for handheld devices, Class files, Compilation process

**Module 3: Mobile OS and Computing Environment**

**SLE:** Data types, and Operations, conditional statements and loops.

**Module 4: Building Wireless Internet Applications and Markup Languages**
Thin client overview: Architecture, the client, Middleware, messaging Servers, Processing a Wireless request, Wireless Applications Protocol (WAP) Overview, Wireless Languages: Markup Languages, HDML, WML, HTML, VoiceXML.

**SLE:** cHTML, XHTML, servlets, JSP, spring, Java collections, JDK.

**Module 5: J2ME**
Introduction, CDC, CLDC, MIDP; Programming for CLDC, MIDlet model, Provisioning, MIDlet life-cycle, Creating new application, MIDlet event handling, GUI in MIDP, Low level GUI Components, Multimedia APIs; Communication in MIDP.

**SLE:** Security Considerations in MIDP.

**Text Books:**

**Reference books:**

**Wireless Networks (3:0:0)**

<table>
<thead>
<tr>
<th>Sub Code: EC8E503</th>
<th>Credits: 3</th>
<th>SEE Hrs: 3</th>
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<tr>
<td><strong>Hrs./week:</strong> 3</td>
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**Course Outcomes:**

On successful completion of the course, the students will be able to:

1. To learn the basic architecture of GSM and CDMA.
2. To have an understanding of wireless protocols.
3. To examine the various Wireless Networks like LAN, WAN, PAN.
4. Describe and compare Broadband Satellite and Microwave Systems.
Module 1: Evolution of Wireless Networks
Review of cellular standards, migration and advancement of GSM architecture and CDMA architecture

7 Hrs.

SLE: Long Term Evolution (LTE) telecommunication technology, IEEE 802.16 WMAN’s.

Module 2: Wireless Protocols
Mobile network layer- Fundamentals of Mobile IP, data forwarding procedures in mobile IP, IPv4, IPv6, IP mobility management, IP addressing - DHCP, Mobile transport layer-Traditional TCP, congestion control, slow start, fast recovery/fast retransmission.

8 Hrs.

SLE: classical TCP improvements Indirect TCP, snooping TCP, Mobile TCP

Module 3: Wireless LANs /IEEE 802.11x:
Introduction, wireless LAN Network components and standards, IEEE 802.11 design issue, design requirements of WLAN, network architecture, MAC layer operations, higher rate standards, wireless LAN security, WLAN applications.

7 Hrs.

SLE: WAVE (Vehicular Environments), WLAN Hardware.

Module 4: Wireless PANs/IEEE 802.15x:
Introduction, wireless PAN architecture, WPAN components, technologies and protocols, Bluetooth (IEEE 802.15.1), Bluetooth Link Controller basics, IEEE 802.15.1 protocols and Host Control Interface, standards, WPAN applications.

8 Hrs.

SLE: Zigbee, WPAN applications.

Module 5: Broadband Satellite and Microwave Systems:
Introduction, line-of sight propagation, fundamentals of satellite systems, broadband satellite networks.

7 Hrs.

SLE: Microwave Internet or Wireless Access (WLA), Satellite Ventures and Future Prospects.

Textbook:

Reference Books:

LOW POWER VLSI DESIGN (3:0:0)

Sub. Code: EC8E601 CIE: 50% Marks

Hrs/week: 3 SEE: 50% Marks

SEE Hrs: 3 Max Marks: 100
Course Outcomes:

At the end of the course the student should be able to:

1. Identify the source of power dissipation in VLSI Circuits.
2. Understand the power optimization at circuit and logic level.
3. Applying the power optimization approaches to VLSI architecture and systems.
4. Illustrate the different techniques involved in special circuits like memory, adder, and multiplier with reference to speed and power
5. Analyze various approaches of power dissipation at different levels of abstraction through simulation for power efficient circuit design

Module 1: Device & Technology Impact on Low Power:

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation. 08Hrs

SLE: Physics of power dissipation in CMOS devices, Low power figure of merits

Module 2: Low Power Design at Circuit level:

Transistor and Gate sizing, Equivalent pin ordering, special latches and Flip Flops, network restructuring and reorganization, low power digital cell library.

Low Power Design at logic level: Gate reorganization, signal gating, logic encoding, state machine encoding. 09Hrs

SLE: Precomputation logic, adjustable device threshold voltage

Module 3: Low Power Architecture and systems:

Power and performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation

Algorithmic low power methods: Introduction, design flow, Algorithmic level analysis and optimization. 08Hrs

SLE: Adaptive filtering, power reduction in clock networks

Module 4: Low power Memory Design:

Introduction, sources and reductions of power dissipation in memory subsystems, sources of power dissipation in SRAM, DRAM, low power SRAM and DRAM circuits.

Low power Arithmetic components: Introduction. Circuit design style, adders, multipliers, division. 10Hrs

SLE: Battery aware task scheduling, adiabatic computation

Module 5: Power estimation, Simulation Power analysis:

SPICE circuit simulation, gate level logic simulation, capacitive power dissipation, static state power, gate level capacitance estimation, architecture level analysis, Data Correlation Analysis in DSP Systems. 07Hrs
SLE: Monte Carlo simulation, signal entropy

Text Books:

Reference Books:

Automotive Electronics(3:0:0)

Sub. Code: EC8E602
Hrs./week: 3 Hrs
SEE Hrs : 3
CIE: 50% Marks
SEE: 50% Marks
Max Marks: 100

Course Outcomes:
On successful completion of the course, the students will be able to:
1. Explain the need of electronics in Automobiles.
2. Identify the sensors and actuators used in modern vehicles.
3. Measure and control Electronic Engines.
4. Apply the networking and communication concepts for Automotive systems.
5. Analysis of various battery systems and Diagnostics techniques used in automobiles.
6. Paraphrase the performance and configuration of Electric, Hybrid and Fuel cell vehicles.

Module 1: Introduction to Automotive Systems
Automotive fundamentals overview: four stroke cycle, engine control, ignition system, spark plug, spark pulse generation, ignition timing, drive train, transmission, brakes, steering system, Power Brakes, Anti-Lock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronically controlled suspension, starting system. 8 Hrs.
SLE: Air/fuel management

Module 2: Sensors and Actuators
SLE: Throttle angle sensor and Evaporative emission systems

Module 3: Electronic Engine Control and Automotive Networking
Electronic Engine Control: Engine parameters, variables, engine performance terms, electronic fuel control system, electronic ignition control, idle speed control, air/fuel systems fuel handling, air intake system, Protection, Remote Keyless Entry
Automotive communication/networking: Automotive networking, cross system function, Requirements for bus systems, Classification of bus systems, Applications in the vehicle, Coupling of networks, Examples of networked vehicles. Bus systems: CAN, LIN. 8 Hrs.

SLE: EGR control and MOST bus.

**Module 4: Diagnostics and Battery systems**

**Module 5: Electric and Hybrid Vehicles**

**Text Books:**

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**NANO ELECTRONICS (3:0:0)**

**Sub Code:** EC8E603

**Hrs./Week:** 03 Hrs

**SEE Hrs.:** 03

**Sub Code:** EC8E603

**CIE:** 50% Marks

**SEE:** 50% Marks

**Max.:** 100 Marks

**Course Outcomes:**
On successful completion of the course the students will be able to:

1. Apply the concepts of nanotechnology and new trends in microelectronics and optoelectronics.
2. Understand the basic concepts of nano-electronic devices.
3. Demonstrate the Fabrication process flow of nano-devices.
5. Apply the basic concepts of Quantum mechanics.
Module 1: Introduction to nanotechnology

Introduction to nanotechnology, Impacts, Limitations of conventional microelectronics, Trends in microelectronics and optoelectronics. Classification of Nanostructures, Low dimensional structures Quantum wells, wires and dots, Density of states and dimensionality. Basic properties of two-dimensional semiconductor nanostructures, square quantum wells of finite depth, parabolic and triangular quantum wells Quantum wires and quantum dots, carbon nanotube, graphene

SLE: Mesoscopic physics, trends in microelectronics and optoelectronics, Quantum mechanical coherence

8 hrs

Module 2: Fabrication methods

Introduction to methods of fabrication of nano-layers, different approaches, Formation of Silicon Dioxide- dry and wet oxidation methods. Fabrication of nanoparticles- grinding with iron balls, laser ablation, reduction methods, sol gel, self-assembly, precipitation of quantum dots.

SLE: Fabrication Process Steps in MOSFET

8 hrs

Module 3: Characterization of nanomaterials


SLE: X-Ray Diffraction analysis, PL & UV Spectroscopy

8 hrs

Module 4: Introduction to Quantum mechanics

Two-dimensional electronic system, two-dimensional behaviour, MOSFET structures, Heterojunctions, Quantum wells, modulation doped quantum wells, multiple quantum wells

SLE: The concept of super lattices- Kronig - Penney model of super lattice.

Module 5: Nanoelectronics devices

Nanoelectronics devices- MODFETS, heterojunction bipolar transistors Resonant tunnel effect, RTD, RTT, Hot electron transistors Coulomb blockade effect and single electron transistor, CNT transistors Heterostructure semiconductor laser Quantum well laser, Quantum well optical modulator, quantum well subband photo detectors, principle of NEMS.

SLE: 

8 hrs
SLE: quantum dot LED, quantum dot laser

Text Book:

Reference Books:

Reconfigurable Computing(3:0:0)

Sub Code: EC8E60X
Hrs./Week: 03 Hrs
SEE Hrs.: 03
CIE: 50% Marks
SEE: 50% Marks
Max.: 100 Marks

Course Outcomes:
On successful completion of the course the students will be able to:
1. Understand the fundamental principles and practices in reconfigurable architecture.
2. Simulate and synthesize the reconfigurable computing architectures.
3. Illustrate the FPGA design principles, and logic synthesis.
4. Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
5. Design digital systems for a variety of applications on signal processing and system on chip configurations.

Module-1: Introduction to Reconfigurable Computing:

SLE: Reconfigurable Logic Co-processor

Module-2: Languages, Compilation and Implementation:

**SLE: Debugging Reconfigurable Computing Applications**

**Module-3: Synthesis, Placement and on-line communication:**
High Level Synthesis for Reconfigurable Devices: Modelling, Temporal Partitioning Algorithms, TEMPORAL PLACEMENT: Offline and Online Temporal Placement, Managing the Device’s Free Space with Empty Rectangles, Managing the Device’s Occupied Space, NoC, Dynamic NoC.  

**SLE: Communication over third party**

**Module-4: Partial Reconfiguration Design:**

**SLE: Enhancement in the Platform Design**

**Module-5: Signal Processing Applications:**
Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution.  

**SLE: SOPC**

**Text Books:**


**Reference Books:**


**Agenda 3: Any other academic matter**

MoM

Following were the suggestions given by the BoS members:
General Comments:

6. In 8th semester all members suggested to have one stream of electives for students.
7. Since 7th semester has Mixed Mode VLSI design laboratory, swap wireless communication as elective and Mixed Signal design as Core course.
8. Suggested to introduce courses like Mobile hazard, Fundamentals of mobile communication, health hazards, Analog and Digital communication, Microprocessor as open elective.
9. BoS suggested to relook on CO’s.
10. BoS members approved following new electives for 7th semester:
    a. System Verilog.
11. BoS members approved following new electives for 8th semester:
    a. Reconfigurable computing.
12. BoS members approved following open Elective:
    a. FPGA based Embedded Systems.
13. Dr. Kanmani B commented on L:T:P:S structure as VTU has only L:T:P structure.
    a. Justification: NBA committee suggested to have SLE components to achieve PO12(Life Long Learning). So, Institute emplaced compulsory SLE component from 2014 academic year.

Antenna and Microwave:

1. Matlab need to be introduce for coding part for better understanding.
2. Reframe SLE components like introduce Regulations by India, coding for dipole antenna equations.

Wireless Communication:

1. GSM and CDMA is absolute, so suggested to remove and introduce advance topics.
2. Too difficult to understand OFDMA as SLE, so move to regular component. And also introduce some simulation part for OFDMA.
3. Move LTE as SLE instead of OFDMA in module-5.
4. Merge module 3 & 4 and introduce MIMO in detail as module 4.
5. NOMA is good as SLE but after CDMA and OFDMA only.
6. Book named “LTE for UMTS: Evolution to LTE-Advanced” by Harri Holma can be introduced for LTE component in 5th module.

Optical Fiber Communication:

1. Suggested to Interact with BSNL RTTC Mysore to frame a component as a part of course.

Multimedia Communication:

1. Haffman code, Lossy and Lossless compression and EZW should not be SLE component.
2. Move Digitalization principles from SLE to regular component.
3. Encourage students to have some publications.
4. Introduce an experiment to capture their own face and apply some of the techniques studied in this course.
Network Security:

1. In module 1, try to teach three or more technique in depth.
2. Mention applications of AES, DES with respect to current technologies like IoT.
3. Introduce topics like storage complexity for advance computations and privacy preservations.
4. Encourage students to explore Google and amazon cloud with reference to cyber security.

System Verilog:

1. In future introduce Verilog and System Verilog as one course.
2. Encourage students to have design and implementation.

RF Electronics:

1. Remove manipulate word in CO4.
2. Co’s need to reframe.
3. Try to reduce 12 hours in module-1.
4. Introduce super heterodyne and CDMA receiver as SLE in module-5 rather than Low-IF Receivers.

Mixed Signal Design:

1. Relook into Co’s
2. Add advanced topics related to DAC and ADC
3. More emphasis on mathematical model.

Speech Processing:

1. Remove manipulate word in CO2.
2. Co’s need to reframe.
3. Add more hands on and realization.

FPGA based Embedded Systems:

1. Need to rethink as open elective but can be introduced as department elective.
2. Suggested to generalize the course and offer as open elective.

Pattern Recognition and Machine Learning

1. SLE component of Module 1 is similar to Module-2.
2. Remove clustering using Minimum spanning tree.
3. Suggested not to use built in functions for any algorithms while practicing coding part.

Artificial Intelligence:

1. Dr. Naveen M B appreciated the SLE component “Chinese room” of module-1.
2. Suggested to frame Pattern Recognition and Machine Learning of 7th semester and Artificial Intelligence of 8th semester collaboratively.
3. Dr. Kanmani B suggested to rename Chinese room.

**Signal Processing and Machine learning:**

1. BoS members approved to rename Advance Signal Processing as “Signal Processing and Machine learning”
2. Need to change/reframe the CO and rename word manipulate.
4. Approved the title change from “Speech processing” to “Speech Processing and Machine Learning”

**Satellite communication:**

2. In CO3 kepler should be replace with Kepler.
3. Introduce Satellite communication in 5G as a SLE component.

**Mobile Communication:**

1. Remove WiMAX and introduce Wi-Fi.
2. Remove Symbian, WinCE, Palm OS and introduce Android.

**Wireless Networks:**

1. Minimize overlap as per the group.
2. WiMax replace with WiFi and can include IoT related wireless networks.